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(54) METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

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(57) Abstract:

PROBLEM TO BE SOLVED: To form a multi-level wiring layer of dual damascene structure effectively using a low permittivity film in a via contact layer or a wiring layer.

SOLUTION: After a multilayer structure of organic films 14 and 18, and organic SOG films 16 and 20 are formed on a substrate, a silicon oxide film becoming a CMP stopper layer, or an organic SOG film and a silicon nitride film becoming an etching film are formed. Subsequently, a wiring pattern is formed on the silicon nitride film using a resist mask and the resist is ashed. Thereafter, SOG is applied for the purpose of planarization and the effect of level different is eliminated. Furthermore, an SOG material is admixed with resin absorbing the exposure wavelength so that a good resolution can be attained. Contact holes are then patterned and the silicon oxide film, organic films and silicon oxide film are etched sequentially. Finally, the silicon oxide film and the organic films are etched using the silicon nitride film as a mask.